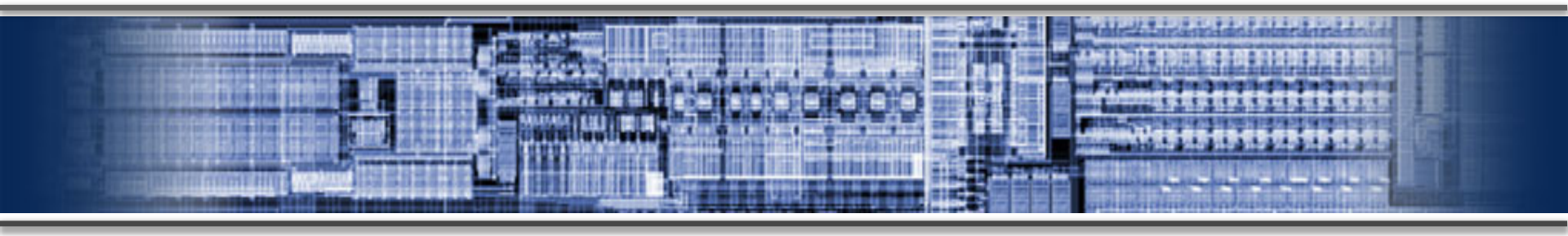


High Performance PLL Design in TSMC 5nm FinFET Process

Randy Caplan

Executive Vice President & Co-Founder, Silicon Creations

June 25, 2018

Outline

- Silicon Creations introduction
- Scaling PLLs to 5nm – what changes?
- 7nm Simulation – Silicon correlations
- Summary

Silicon Creations Overview

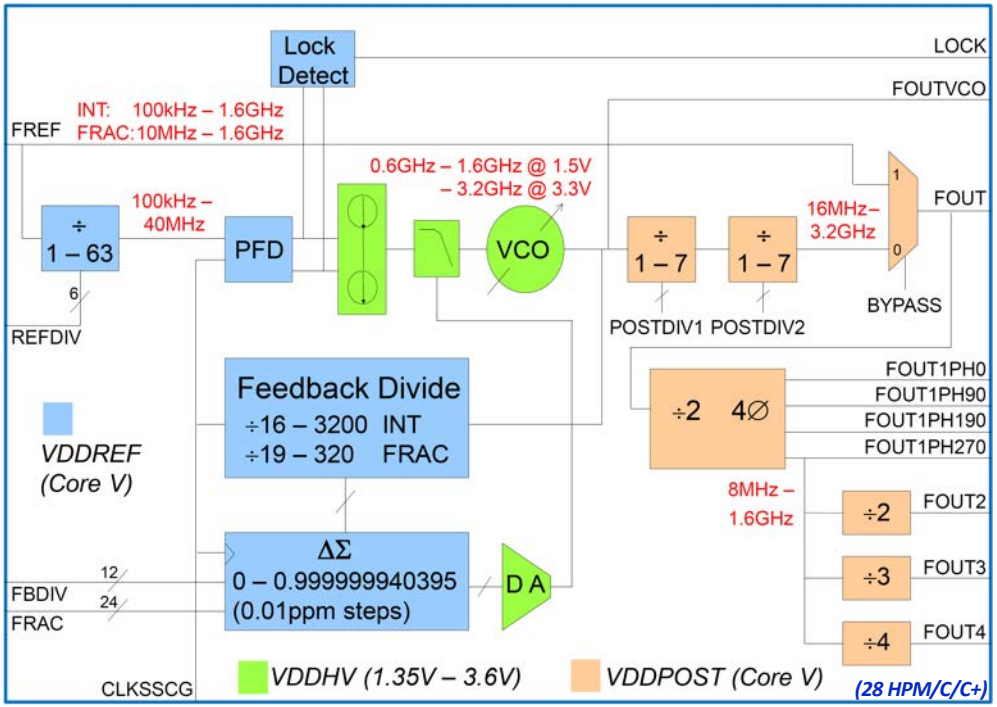
- IP provider of PLLs, Oscillators and High-speed Interface
- Founded 2006 – self-funded, profitable and growing
- Design offices in Atlanta and Krakow, Poland
- High quality development, award winning support
- >160 customers (>60 in China)
- Mass production from 7nm to >180nm, 5nm coming soon

Awards for quality & support

- 2017
  - Audience choice paper, USA OIP
  - Mixed-Signal IP Partner of the year
- 2014
  - Best Emerging IP vendor

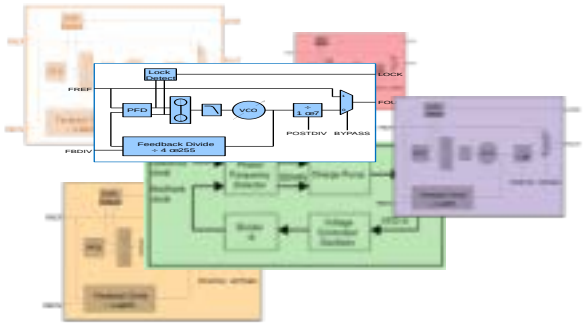
Fractional Ring PLL

- "One-Size-Fits-All" Synthesizer: flexibility reduces risk
  - Any crystal; <0.01ppm frequency step
- Programmable Power – Jitter Optimization
  - < 1mW
  - Long Term Jitter < 5ps RMS
- Production from 7nm, 5nm in development
- Derivative PLLs for
  - Core voltage only
  - Integer-only
  - Low area
  - Ultra-low jitter
  - Ultra-low power

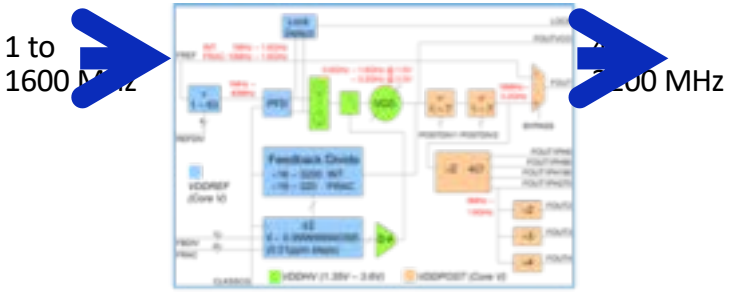


Why our Fractional PLL?

Competitors



Silicon Creations



Risky & expensive

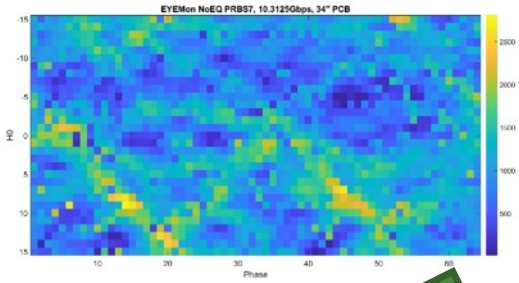
- Built new each time
- Narrow input/output ranges
  … need new masks to adjust
- Buy a new IP for every clock

Lower risk & lower cost

- Predictable, measured
- Wide range, programmable power-performance tradeoffs
- One PLL, many applications – save $, ¥, €
- Best support

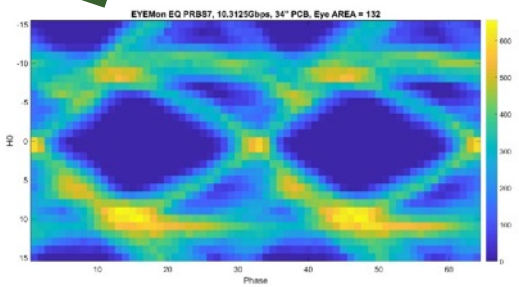
Multi-Protocol SerDes PMA

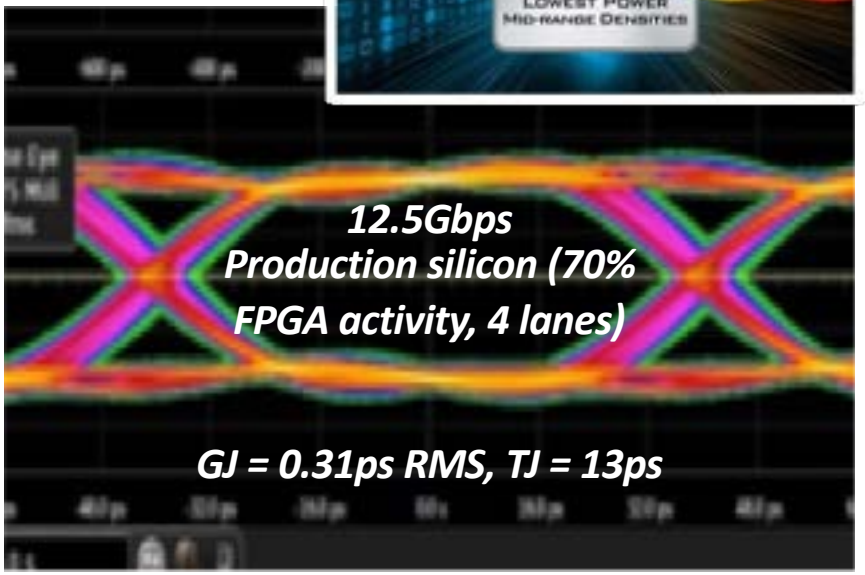
- 0.25 – 16Gbps SerDes PMA (28LP, 40 LP, 12/16FFC soon)
- Low Power (mW/Gbps/lane): SR <4.5mW, LR <8.6mW
- Jitter cleaner Tx Ring PLL → Low Area



(10.3Gbps, 25dB channel loss)

5-tap DFE + CTLE + Eye monitor + Adaptive Eq.
→ **>30 protocols**





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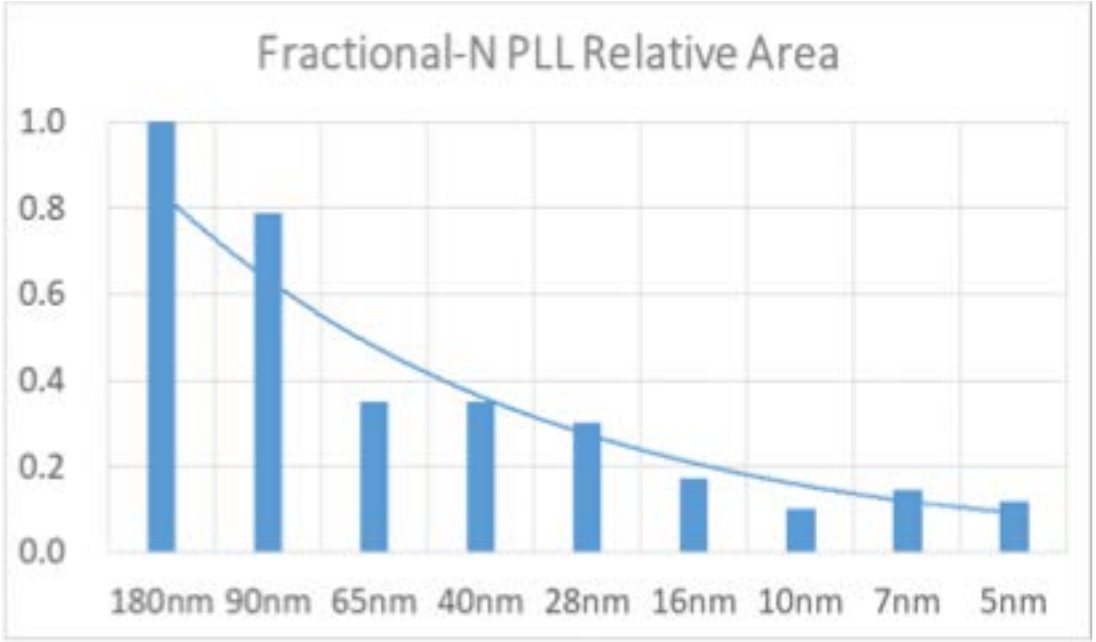
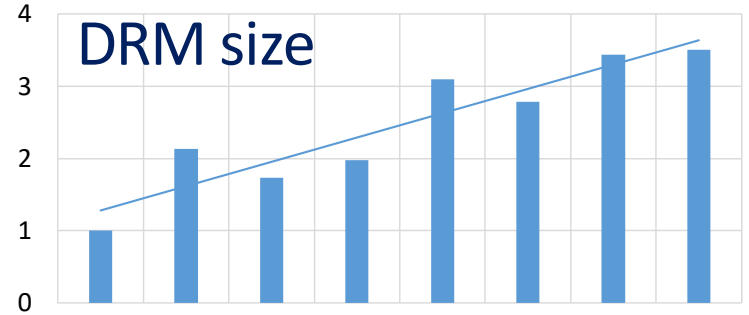
Analog scaling to 5nm

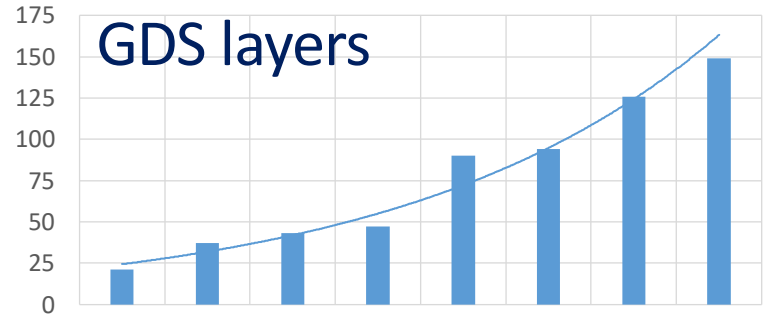
- Analog noise relates to kT/C, so area should scale with capacitance area
- It does! Analog scales, but less than digital
- From 180nm to 5nm:
  - Digital scaling is ~800:1
  - Analog scaling is ~8:1

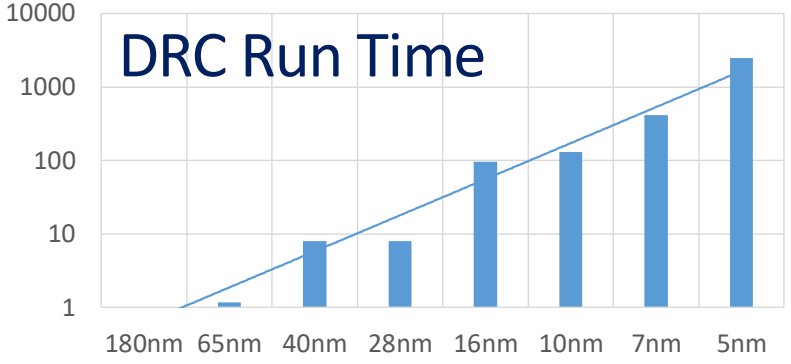


5nm Process Complexity

- DRM size
  - From 180nm to FinFET, the # DRM pages increased 3.5x
- GDS layer count
  - Increased 7x
- Relative DRC Run Time
  - More complex rules, more fill geometries
  - Run times compared to 28nm:
    - 16nm FinFET are ~10x longer
    - 7nm FinFET are ~50x longer
    - 5nm FinFET are ~300x longer

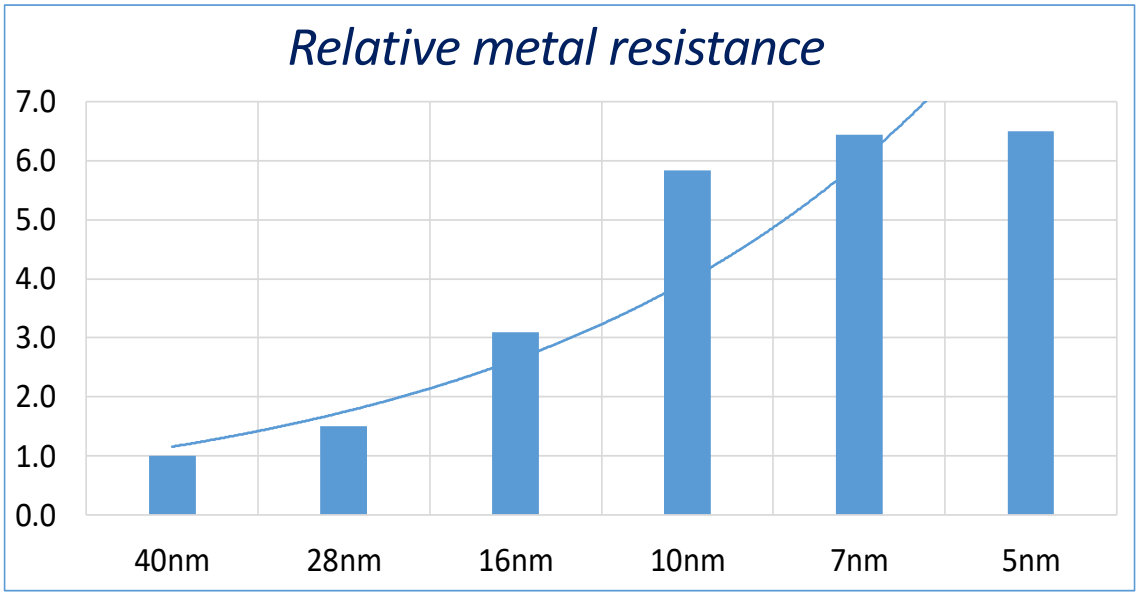






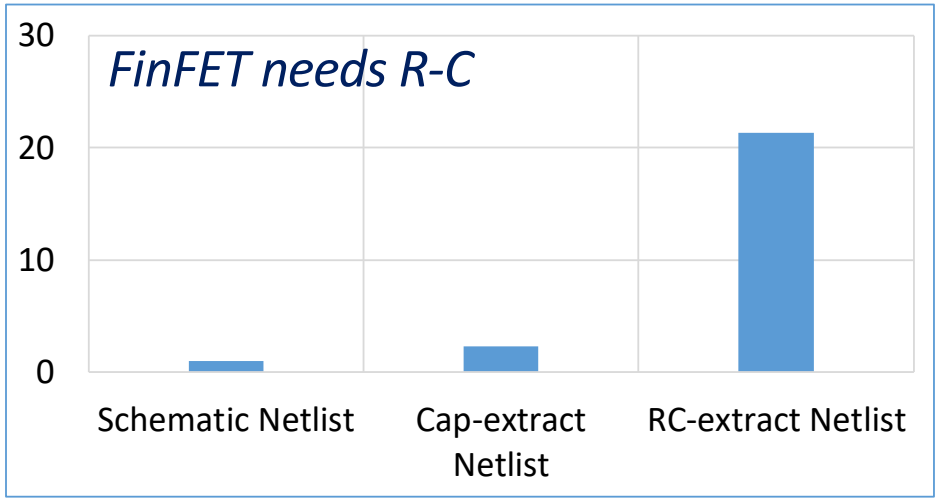
Wire resistance challenge

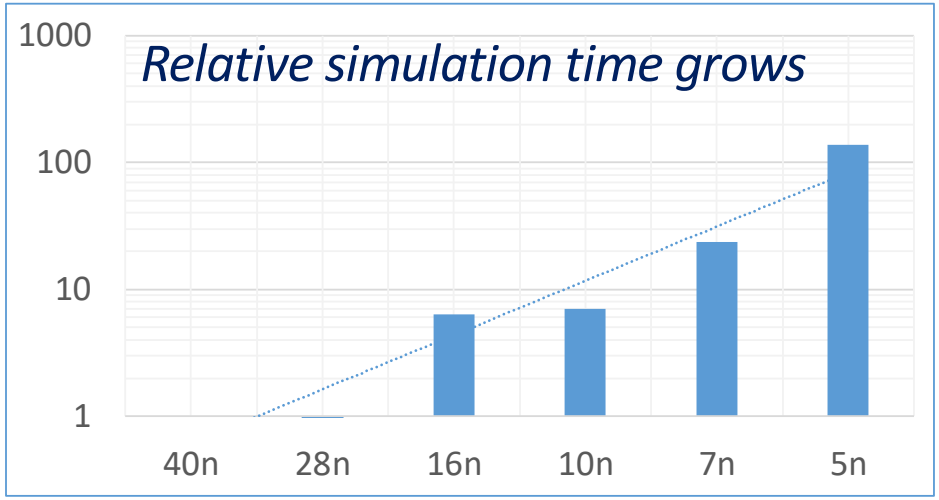
- Interconnect resistance is climbing quickly!
- Extraction and post extract simulations are becoming more important
- From 40nm to 5nm/7nm, wire resistance (Ω/sq) has risen ~6.5x
- Designs are increasingly difficult to verify due to the need for simulation of distributed RC parasitics



5nm Simulation Time

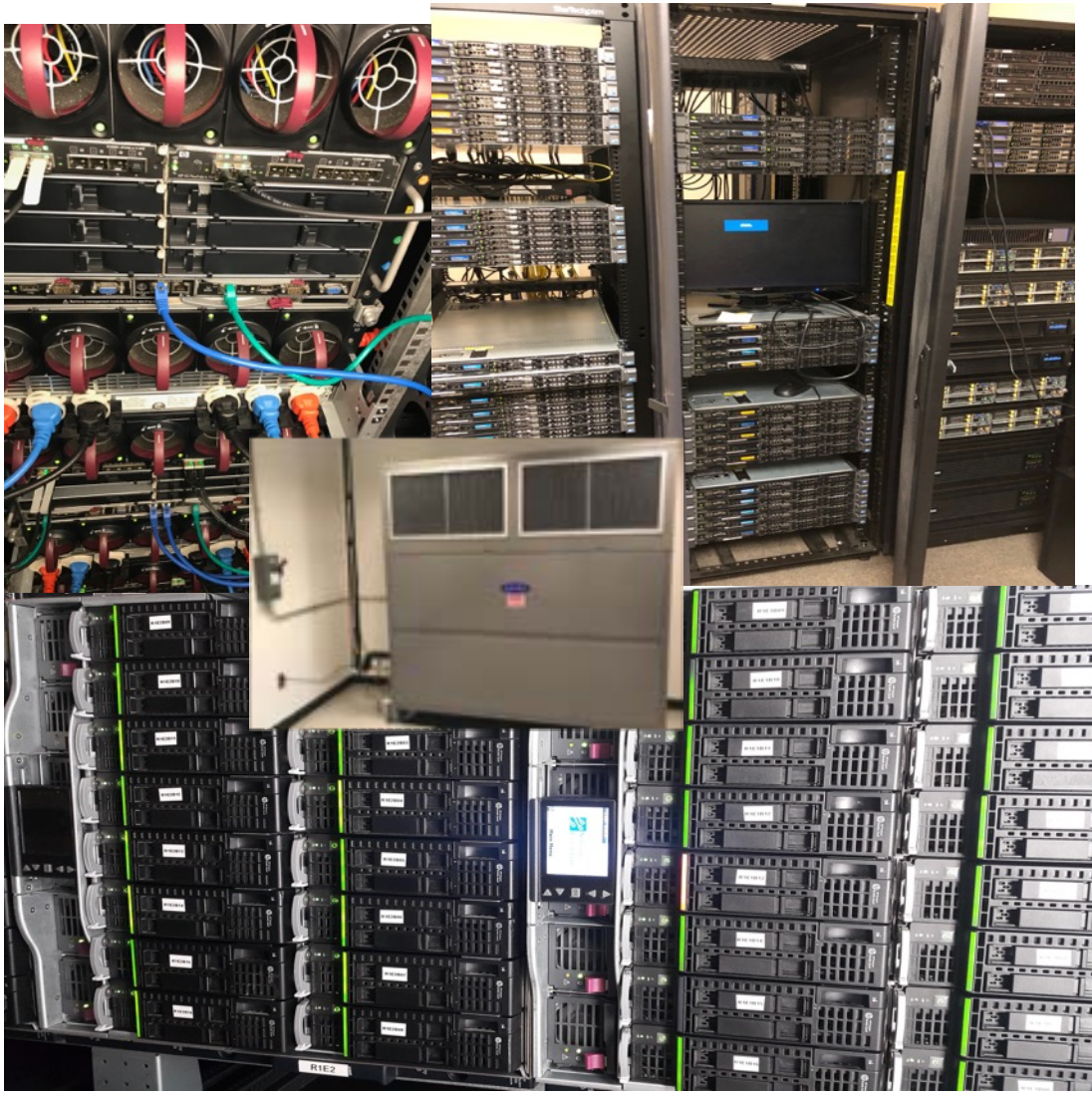
- Schematic sims are out, distributed C-C and R-C extracted simulations are needed
- Translates to Higher development costs:
  - Longer development cycles
  - Need parallel simulation and more CPU's
  - Need more EDA licenses





5nm Computing Solution

- Distributed computing farm
  - 2200+ CPU cores
  - 15TB+ RAM
- 1200 Simulation licenses
  - 200+ 16-core extracted sims
  - 300+ 4-core extracted sims
- Dedicated Calibre machines
  - Intel i9-7980XE 4.8GHz
    - World's fastest 18-core machine
  - CPU de-capped, water-cooled
  - 4x16GB DDR4 RAM
- Carrier 15 Ton Cooling Units
  - >50kW Capacity
- 140 kW at full capacity!



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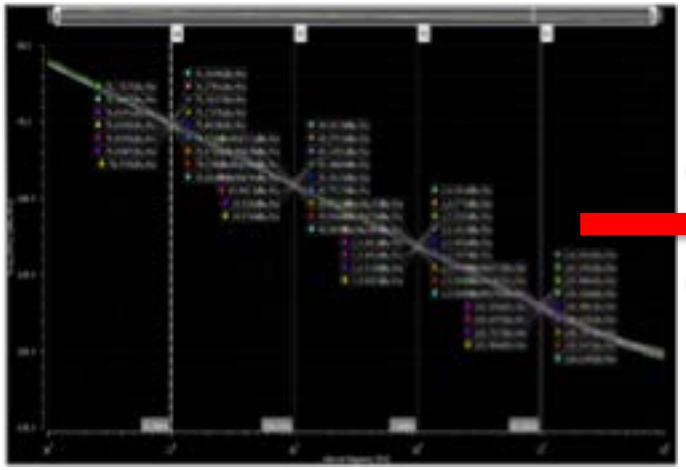
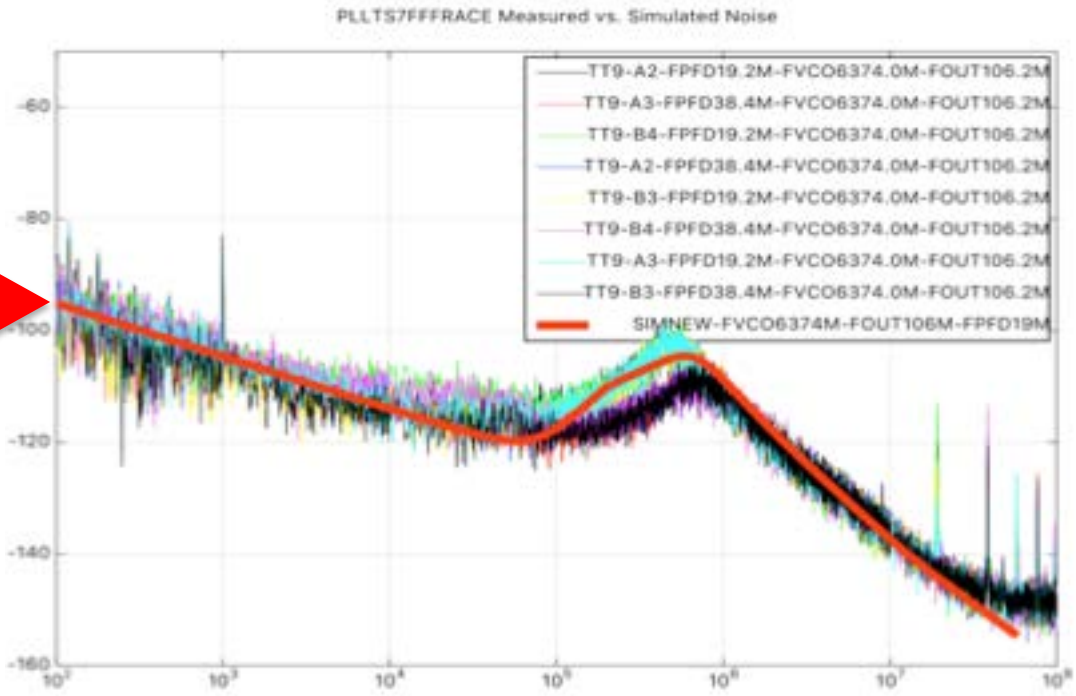
Simulation = 7nm Silicon

Excellent correspondence between Mentor AFS derived phase noise and measured performance



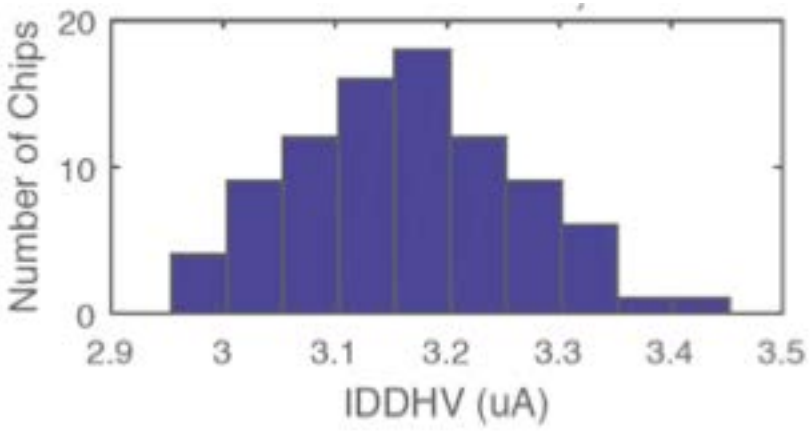
AFS PSS + Pnoise
(VCO, Charge pump)



7nm IoT PLL Power

- **Simulation**
  - Mean=3.02uA
  - Stddev=1.5%
- **Measurement**
  - Mean=3.15uA
  - Stddev=1.6%

Measured Current Distribution



Summary

- Silicon Creations provides PLLs, interfaces such as LVDS and SerDes to 25Gbps
- Market leader in PLLs – already in production in 7nm, well underway in 5nm
- Designing in FinFET brings many challenges including simulation complexity and runtime; need to pay close attention to parasitics, proximity and matching, and balance accuracy and design time
- 5nm is significantly more complex than 16nm/12nm, but no new techniques are needed; our PLL circuit topology has worked from 180nm to 5nm